Course Type	Course Code	Name of Course	L	T	P	Credit
DE	NECD508	Test and Verification of VLSI Circuits	3	0	0	3

Course Objective
With this course students will learn the most recent, yet fundamental, VLSI test and verification principles along with design for testability (DFT) architectures in an effort to help them design better quality products that can be reliably manufactured in large quantity.
Learning Outcomes
Upon successful completion of this course, students will: •Acquire knowledge about manufacturing defects, fault modeling and collapsing.•Model and simulate different types of faults in digital circuits at various levels of abstraction.•Critique and compare various ATPGalgorithms for combinational and sequential circuits.•Acquire knowledge about various verification techniques.

Module No.	Topics to be Covered	Lecture Hours	Learning Outcome
1	Introduction to VLSI testing and verification, Defects and Faults, Functional and structural testing, Physical faults and their modeling, Fault Coverage, Single and multiple stuck-at fault model, Fault collapsing, Fault Equivalence and dominance, Checkpoint theorem, Delay fault testing, Iddqtesting.	9	Acquire an understanding of role of VLSI test and verification, concept of faults and various test methodologies existing for digital VLSI circuits.
2	Fault simulation, Algorithms for fault simulation: Serial, parallel, deductive and concurrent techniques; Critical path tracing.	5	Learnabout various fault simulation algorithms, their merits and demerits.
3	Test generation for combinational circuits: Boolean difference, D-algorithm, PODEM, etc.; Exhaustive, random and weighted test pattern generation; aliasing and its effect on fault coverage.	6	Learnabout various test generation algorithms for combinational circuits, their merits and demerits.
4	Test pattern generation for sequential circuits: ad-hoc and structured techniques; scan path and LSSD, boundary scan. Design for testability.	5	Learnabout various test generation algorithms for sequential circuits, and design for testability (DFT) architectures.
5	Built-in self-test techniques, System-on-chip (SoC) testing, Low-power testing.	5	This unit helps the students to learnBuilt-in self-test (BIST) techniques, methodologies for SoC testing and low-power testing.
6	PLA testing: cross-point fault model, test generation, easily testable designs; Memory testing: permanent, intermittent and pattern-sensitive faults; test generation.	6	This unit helps the students to learnvarious modeled faults in PLA and memory along withtheir test methodologies.
7	Design verification techniques based on simulation, analytical and formal approaches. Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking. Hardware emulation.	6	This unit introduces the role of design verification and various approaches used for verification.
	Total	**42**	

Textbook:

1. M.L.Bushnell andV.D.Agrawal,"Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2009.
2. William K Lam, "Hardware Design Verification: Simulation and Formal Method-Based Approaches", Prentice Hall Modern Semiconductor Design Series, 2005.

Reference Books:

1. M. Abramovici, M. A. Breuer and A. D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2. N. K Jha and S. Gupta, "Testing of Digital Systems", Cambridge University Press, 2003.
3. P.K.Lala,"DigitalCircuitTestingandTestability",AcademicPress,2002.
4. A. L. Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.